

FIG. 1

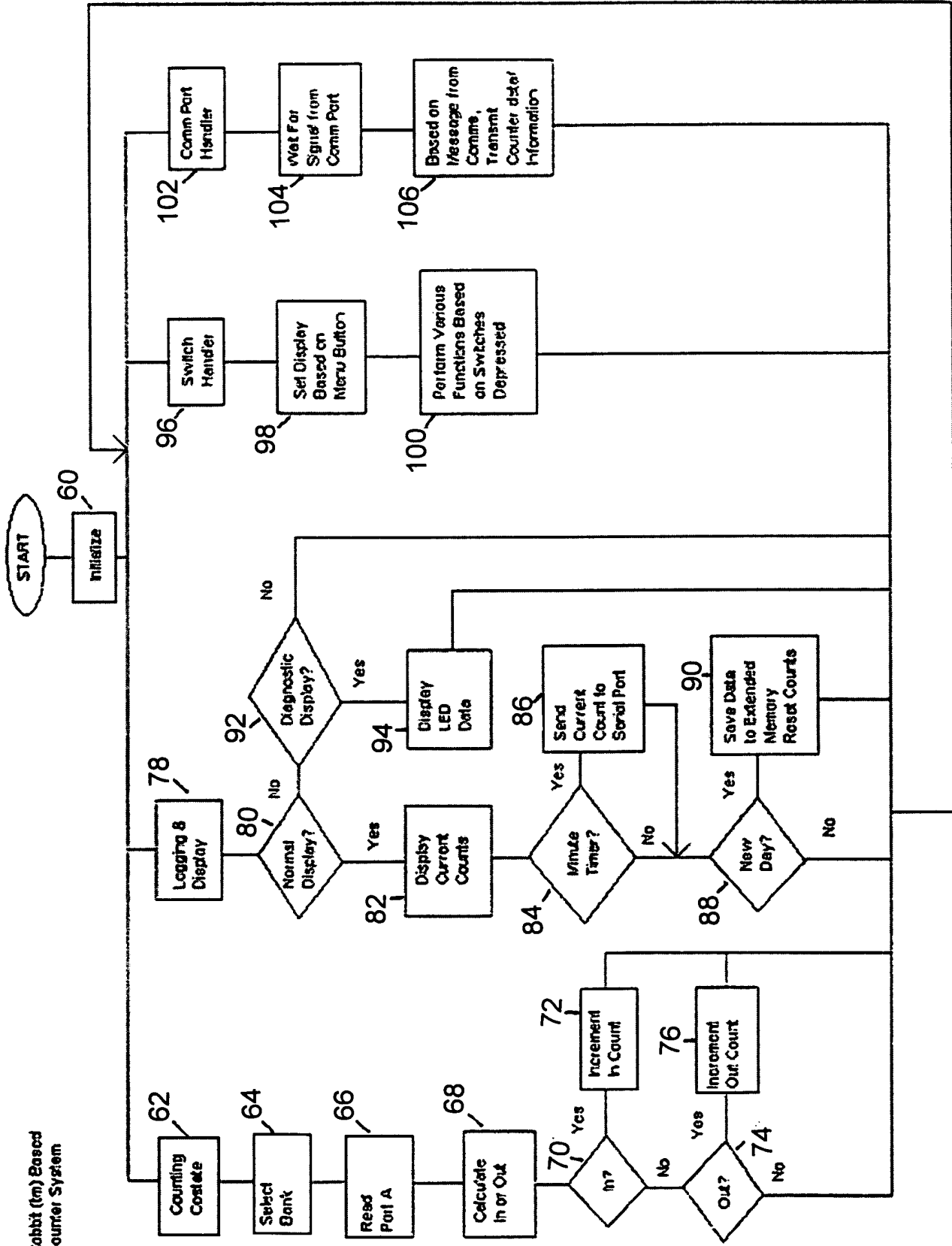


FIG. 2

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Write to out port to select counter bank
WrPortI(PBDR, &PBDRShadow, bank<<6);

count = RdPortI(PADR);

for (i=0; i<4; i++) {
    j = bank*4 + i;
    temp = (count>>(2*i)) & 0x03; // get this channel's bits
    if ((channel[j] & 0x03) != temp)
    {
        if (((channel[j] & 0x03) == 0x00) && ((temp<<2) == (channel[j] & 0x0C))) // bulking bee
            // pop the stack
            channel[j] = (channel[j] >> 2) | 0xC0;
        else
        {
            // analysis
            if ((temp == 0x03) && (channel[j] == 0xD2)) {in++; timeins[period] ++;} // we got an in!
            if ((temp == 0x03) && (channel[j] == 0xE1)) {out++; timeouts[period] ++;} // we got an out!
            // push new value onto "stack"
            channel[j] = ((channel[j] & 0x3F) << 2) | temp;
        }
        // less rigorous method, for fast bees and slow detectors
        if (channel[j] == 0xD3) {in++; timeins[period] ++;}
        if (channel[j] == 0xE3) {out++; timeouts[period] ++;}
    }
}
} // end for i loop
} // end bank loop
loopert++; // cycle counter
} // end costate

```

FIG. 3